CLAIMS

What is claimed is:

1. A semiconductor package comprising:

at least first and second semiconductor chips;

a substrate having opposing first and second surfaces and a through hole extending through the substrate between the first and second surfaces;

a first conductive circuit pattern disposed on the first surface of the substrate and a second conductive circuit pattern disposed on the second surface of the substrate;

the first semiconductor chip having opposing active and inactive surfaces, the first semiconductor chip being at least partially disposed within the through hole, the active surface of the first semiconductor chip being electrically connected to the first conductive circuit pattern;

the second semiconductor chip having opposing active and inactive surfaces, the second semiconductor chip being at least partially disposed within the through hole, the active surface of the second semiconductor chip being electrically connected to the second conductive circuit pattern;

an encapsulant material disposed over at least a portion of the first semiconductor chip, over at least a portion of the second semiconductor chip, and within the through hole.

2. The semiconductor package of claim 1, wherein the first semiconductor chip is entirely disposed within the through hole.

3. The semiconductor package of claim 1, wherein the first and second semiconductor chips are both entirely disposed within the through hole.

4. The semiconductor package of claim 1, wherein the active surface of the second semiconductor chip and the second surface of the substrate lie in a common horizontal plane.

5. The semiconductor package of claim 1, wherein the inactive surface of the first semiconductor chip is adhered to the inactive surface of the second semiconductor chip by an adhesive.

6. The semiconductor package of claim 1, wherein the inactive surface of the first semiconductor chip comprises a smaller area than the inactive surface of the second semiconductor chip.

7. The semiconductor package of claim 1, wherein the inactive surface of the first semiconductor chip comprises an area equal in size or greater than the inactive surface of the second semiconductor chip.

8. The semiconductor package of claim 1, wherein the second conductive circuit pattern includes a plurality of lands.

9. A semiconductor package comprising:

a substrate having opposing first and second surfaces and through hole extending through the substrate between the first and second surfaces;

a conductive circuit pattern disposed on the first surface of the substrate;

a first semiconductor chip having opposing active and inactive surfaces, the first semiconductor chip being at least partially disposed within the through hole, the active surface of the first semiconductor chip being electrically connected to the conductive circuit pattern;

a second semiconductor chip having opposing active and inactive surfaces, the second semiconductor chip being at least partially disposed within the through hole, the active surface of the second semiconductor chip being electrically connected to the conductive circuit pattern, wherein the inactive surface of the first semiconductor chip is mounted on the active surface of the of the second semiconductor chip and the active surfaces of the first and second semiconductor chips are oriented in a same direction;

an encapsulant material disposed over at least a portion of the first semiconductor chip, over at least a portion of the second semiconductor chip, and within the through hole.

10. The semiconductor package of claim 9, wherein the inactive surface of the first semiconductor chip has a smaller area than the active surface of the second semiconductor chip.

11. The semiconductor package of claim 9, wherein the second semiconductor chip is entirely disposed within the through hole.

12. The semiconductor package of claim 9, wherein both the first and the second semiconductor chips are entirely disposed within the through hole.

13. The semiconductor package of claim 9, wherein the active surfaces of the first and second semiconductor chips are oriented in a same direction as the first surface of the substrate.

14. The semiconductor package of claim 9, wherein the first and second semiconductor chips are a same size or wherein the first semiconductor chip is larger than the second semiconductor chip.

15. A semiconductor package, comprising:

a metal core having a first surface and an opposing second surface;

a first dielectric layer disposed on the first surface of the metal core and a second dielectric layer disposed on the second surface of the metal core, the first dielectric layer having a first conductive circuit pattern disposed thereon and the second dielectric layer having a second conductive circuit pattern disposed thereon, with the first dielectric layer having a first recess formed therein such that the first surface of the metal core is exposed through the first recess, and with the second dielectric layer having a second recess formed therein such that the second surface of the metal core is exposed through the second recess;

a first semiconductor chip having opposing active and inactive surfaces, wherein the inactive surface of the first semiconductor chip is mounted on the metal core first surface and within the first recess, the active surface of the first semiconductor chip being is electrically connected to the first conductive circuit pattern, and the first semiconductor chip is at least partially within the first recess;

a second semiconductor chip having opposing active and inactive surfaces, wherein the inactive surface of the second semiconductor chip is mounted on the metal core second surface and within the second recess, the active surface of the second semiconductor chip is electrically connected to the second conductive circuit pattern, and the second semiconductor chip is at least partially within the second recess;

a first encapsulant at least partially encapsulating the active surface of the first semiconductor chip and a second encapsulant at least partially encapsulating the active surface of the second semiconductor chip; and

at least one electrically conductive via extending the metal core and electrically connecting the first and second conductive circuit patterns.

16. The semiconductor package of claim 14, wherein the inactive surfaces of the first and second semiconductor chips are of same or different sizes.

17. The semiconductor package of claim 14, wherein the second conductive circuit pattern includes a plurality of lands, or further comprising a plurality of conductive

balls, each of the conductive balls being electrically connected to a corresponding one of the lands.

18. A semiconductor package comprising:

a substrate having opposing first and second surfaces and a through hole extending through the substrate between the first and second surfaces;

a conductive circuit pattern disposed on the first surface of the substrate;

a first semiconductor chip having opposing active and inactive surfaces, wherein the first semiconductor chip is at least partially disposed within the through hole, the active surface of the first semiconductor chip is electrically connected to the conductive circuit pattern, and the inactive surface of the first semiconductor chip is coplanar with the second surface of the substrate;

a second semiconductor chip having opposing active and inactive surfaces, wherein the second semiconductor chip is at least partially disposed within the through hole, the active surface of the second semiconductor chip is electrically connected to the conductive circuit pattern and to the active surface of the first semiconductor chip, and the inactive surface is coplanar with the second surface of the substrate;

an encapsulant material disposed over at least a portion of the first semiconductor chip, over at least a portion of the second semiconductor chip, and within the through hole.

19. The semiconductor package of claim 18, further comprising:

a plurality of electrically conductive vias extending between the first and second surfaces of the substrate and electrically connected the conductive circuit pattern;

a plurality of lands formed on the second surface of the substrate, each land being electrically connected to at least one of the vias.

20. A stack of semiconductor packages comprising:

at least first and second semiconductor packages;

the first semiconductor package comprising a first substrate having a first surface and an opposite second surface, a through hole between the first and second surfaces, a conductive circuit pattern on each of the first and second surfaces of the first substrate, a first semiconductor chip at least partially within the through hole and in electrical connection with the circuit pattern a second semiconductor chip at least partially within the through hole, and in electrical connection with the circuit pattern;

the second semiconductor package comprising a second substrate and at least a third semiconductor chip connected to the second substrate, wherein a plurality of input/output terminals of the second semiconductor package are electrically connected to the third semiconductor chip, wherein the second semiconductor package is in a stack with the first semiconductor package, and at least some of the input/output terminals of the second package are electrically

connected to the circuit pattern of the substrate of the first semiconductor package.

21. The stack of semiconductor packages of claim 20, wherein the second semiconductor package further comprises a fourth semiconductor chip electrically connected to the input/output terminals.

22. The stack of semiconductor packages of claim 20, wherein an inactive surface of the first semiconductor chip is in a same plane as a major surface of the substrate of the first semiconductor package.

23. The stack of semiconductor packages of claim 20, wherein an active surface of the first semiconductor chip is in a same plane as a major surface of the substrate.

24. The stack of semiconductor packages of claim 20, wherein the first and second semiconductor packages are a same size or a different size.

25. The stack of semiconductor packages of claim 20, wherein active surfaces of the first and second semiconductor chips are of same or different sizes.